FORM PTO-1449

SEVENTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1875.0370000	09/849,537
FIRST NAMED INVENTOR	
Tonglong Zhang	
FILING DATE	ART UNIT
May 7, 2001	2822

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
MC	AA1	5,650,662	07/1997	Edwards *et al.*			
	AB1	5,889,321	03/1999	Culnane *et al.*			
	AC1	5,895,967	04/1999	Steams *et al.*			
	AD1	5,907,189	05/1999	Mertol			
	AE1	5,976,912	11/1999	Fukutomi *et al.*			
	AF1	5,977,633	11/1999	Suzuki *et al.*			
	AG1	6,034,427	03/2000	Lan *et al.*			
	AH1	6,040,984	03/2000	Hirakawa			
	AI1	6,207,467 B1	03/2001	Vaiyapuri *et al.*			
	AJ1	6,278,613 B1	08/2001	Fernandez *et al.*			
MC	AK1	6,313,525 B1	11/2001	Sasano			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

MC	AR	1	Amkor package data sheet, "SuperFC®", from http://www.amkor.com/Products/all_datasheets/superfc.pdf, 2 pages (Jan. 2003).
MC	AS	1	Andros, F., "Tape Ball Grid Array," from Puttlitz, K.J. and Totta, P.A. (eds.), *Area Array Interconnection Handbook*, pp. 619-620, ISBN No. 0-7923-7919-5, Kluwer Academic Publishers (2001).
MC	AT	1	Brofman, P.J. *et al.*, "Flip-Chip Die Attach Technology," Puttlitz, K.J. and Totta, P.A. (eds.), *Area Array Interconnection Handbook*, pp. 315-349, ISBN No. 0-7923-7919-5, Kluwer Academic Publishers (2001).

EXAMINER [signature] DATE CONSIDERED 12/16/04

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	AA2	6,528,869 B1	03/2003	Glenn *et al.*			
	AB2	6,614,660 B1	09/2003	Bai *et al.*			
	AC2	6,617,193 B1	09/2003	Toshio *et al.*			
	AD2	6,657,870 B1	12/2003	Ali *et al.*			
	AE2	6,664,617 B2	12/2003	Siu			
	AF2	6,724,071 B2	04/2004	Combs			
	AG2	6,724,080 B1	04/2004	Ooi *et al.*			
	AH2	2001/0001505 A1	05/2001	Schueller *et al.*			
	AI2	2001/0040279 A1	11/2001	Mess *et al.*			
	AJ2	2002/0171144 A1	11/2002	Zhang *et al.*			
	AK2	2002/0185717 A1	12/2002	Eghan *et al.*			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	2	Freyman, B. and Petrucci, M., "High-Pincount PBGAs," *Advanced Packaging*, pp. 44-46, An IHS Group Publication (May/June 1995).
	AS	2	Ghosal, B. *et al.*, "Ceramic and Plastic Pin Grid Array Technology," Puttlitz, K.J. and Totta, P.A. (eds.), *Area Array Interconnection Handbook*, pp. 551-576, ISBN No. 0-7923-7919-5, Kluwer Academic Publishers (2001).
	AT	2	Harper, C.A. (ed.), *Electronic Packaging And Interconnection Handbook*, Third Edition, pp. 7.58-7.59, ISBN No. 0-07-134745-3, McGraw-Hill Companies (2000).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	2004/0072456 A1	04/2004	Dozier, II *et al.*			
	AB3						
	AC3						
	AD3						
	AE3						
	AF3						
	AG3						
	AH3						
	AI3						
	AJ3						
	AK3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

MV	AR	3	Lin, S. and Chang, N., "Challenges in Power-Ground Integrity," *Proceedings Of The 2001 International Conference On Computer-Aided Design*, pp. 651-654 (November 4-8, 2001).
MV	AS	3	Lloyd, J. and Overhauser, D., "Electromigration wreaks havoc on IC design," *EDN*, pp. 145-148 (March 26, 1998).
MV	AT	3	Song, W.S. and Glasser, L.A., "Power Distribution Techniques for VLSI Circuits," *IEEE Journal Of Solid-State Circuits*, Vol. SC-21, No. 1, pp. 150-156 (February 1986).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						
	AK4						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

MV	AR	4	Tang, K.T. and Friedman, E.G., "Simultaneous Switching Noise in On-Chip CMOS Power Distribution Networks," *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 4, pp. 487-493 (August 2002).
MV	AS	4	Zhao, S. *et al.*, U.S. Patent Application No. 10/870,927, filed June 21, 2004, entitled "Apparatus and Method for Thermal and Electromagnetic Interference (EMI) Shielding Enhancement in Die-up Array Packages".
MV	AT	4	Khan, R. *et al.*, U.S. Patent Application No. 10/952,172, filed September 29, 2004, entitled "Die Down Ball Grid Array Packages and Method for Making Same".

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